In the Claims:

1. (Currently amended) A semiconductor device having a first major surface[[;]] comprising: at least one cell having longitudinally spaced source and drain regions at the first major surface, a source body region at the end of the source region facing the drain region, a drain body region at the end of the drain region facing the source region and a drift region extending from the source body region to the drain body region;

at least one pair of longitudinally spaced insulated gates, one of the pair being adjacent to the source body region and the other of the pair being adjacent to the drain body region, the gates extending longitudinally with longitudinal side walls, the insulated gates being formed in trenches having gate dielectric along the side and end walls and the base of the trench and a gate conductor within the gate dielectric; and

plates adjacent to the drift region for controlling the drift region to carry current flowing between source and drain when the device is switched on and to support a voltage between source and drain when the device is switched off.

2. (Previously presented) A semiconductor device according to claim 1 wherein the source and drain regions are of a first conductivity type and the source and drain body regions are of a second conductivity type opposite to the first conductivity type.

3. (Previously presented) A semiconductor device according to claim 2 wherein the drift region is of the first conductivity type with a dopant concentration in the range of 5×10^{16} cm $^{-3}$ to 5×10^{17} cm $^{-3}$.

4. (Previously presented) A semiconductor device according to claim 1 wherein the plates are insulated conductive potential plates adjacent to the drift region.

5. (Previously presented) A semiconductor device according to claim 4 wherein an insulated conductive potential plate extends from the each of the pair of gates longitudinally towards the other of the pair of gates adjacent to the drift region, each conductive potential plate being in electrical contact with the gate from which it extends.

6. (Previously presented) A semiconductor device according to claim 5 wherein the dielectric along the side wall of the potential plates has a greater thickness than the dielectric along the side wall of the gates.

7. (Previously presented) A semiconductor device according to claim 4 comprising at least one longitudinally extending potential plate between the longitudinally spaced gates and insulated from the longitudinally spaced gates.

8. (Currently amended) A semiconductor device according to claim 1 comprising a ~~81~~ plurality of cells spaced laterally across the first major surface of the substrate alternating with pairs of longitudinally spaced insulated gates.

9. (Currently amended) A semiconductor device according to claim 1 wherein the plates comprise resistive field plates extending longitudinally on either side of ~~the or~~ each cell from a source end adjacent to the source to a drain end adjacent to the drain ~~laterally on either side of the or each cell~~.

10. (Previously presented) A semiconductor device according to claim 9 further comprising a source contact connected in common to the source region or regions and to the source end of the field plate or plates and a drain contact connected in common to the drain region or regions and drain end the field plate or plates.

11. (Previously presented) A semiconductor device according to claim 9 wherein the gate trenches extend from the first major surface to the substrate and the semi-insulating field plates each extend from the first major surface to the substrate.

12. (Previously presented) A semiconductor device according to claim 9 including a plurality of cells and field plates alternating laterally across the first major surface.

13. (Previously presented) A semiconductor device according to claim 1 wherein the gates are arranged within the lateral bounds of each cell.

14. (Currently amended) A semiconductor device according to claim 1 wherein the source body region extends under the source region ~~(22)~~ and the drain body region extends under the drain region.

15. (Currently amended) A semiconductor device according to claim 1 comprising a source contact connected in common to the source and to the source body region and ~~alnd~~ a drain contact connected in common to the drain and the drain body region ~~rrsgion~~.